

A Wide-Band CMOS LC VCO With Linearized Coarse Tuning Characteristics

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Abstract—A pseudo-exponential capacitor bank structure is proposed to implement a wide-band CMOS LC voltage-controlled oscillator (VCO) with linearized coarse tuning characteristics. An octave bandwidth VCO employing the proposed 6-bit pseudo-exponential capacitor bank structure has been realized in $0.18\text{-}\mu\text{m}$ CMOS. Compared to a conventional VCO employing a binary weighted capacitor bank, the proposed VCO has considerably reduced the variations of the VCO gain (K_{VCO}) and the frequency step per a capacitor bank code ($f_{\text{step/code}}$) by 2.7 and 2.1 times, respectively, across the tuning range of 924–1850 MHz. Measurement results have also shown that the VCO provides the phase noise of -127.1 dBc/Hz at 1-MHz offset for 1.752-GHz output frequency while dissipating 6 mA from a 1.8-V supply.

Index Terms—Switched-capacitor array bank, voltage-controlled oscillators (VCOs), wide-band VCO.

I. INTRODUCTION

WIDE tuning range is required in CMOS LC voltage-controlled oscillators (VCOs) for supporting broadband and multiband RF transceivers. One of the most effective way to achieve wide tuning range and low tuning sensitivity at the same time is to use a switched-capacitor array bank while keeping the varactor size small in LC tank [1]–[3]. An auxiliary band switching based on the same switched-capacitor technique can be also useful in extending the tuning range further [4]. When such a VCO having the switched-capacitor bank operates in a phase-locked loop (PLL), coarse tuning is first performed by applying a proper digital code to the capacitor bank and subsequently fine tuning is carried out by applying an analog tuning voltage to the varactor. The coarse and fine tuning sensitivities of VCOs are defined as per-code frequency step ($f_{\text{step/code}}$: the amount of frequency change per a unit capacitor bank code change) and VCO gain (K_{VCO} : the amount of frequency change per tuning voltage change), respectively.

Conventional structure of switched-capacitor array bank is binary-weighted structure. One of the serious and practical issues in this structure is that when the tuning range becomes very wide, this structure easily causes unacceptably large variations in the coarse and fine tuning sensitivities across the tuning range. The huge variations are not desirable for the VCO itself as well as for PLL adopting the VCO. In [5], [6], the varactor size adjustment technique was proposed to reduce the K_{VCO} variation. Nevertheless they employed the conventional binary weighted

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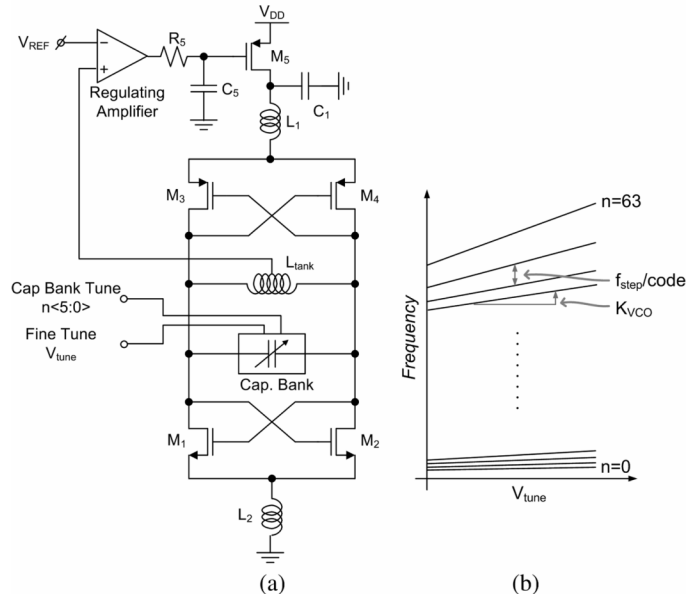


Fig. 1. CMOS LC VCO. (a) Circuit schematic. (b) Typical tuning characteristics.

capacitor bank structure so that their approach would be limited in their effects.

In this paper, the limitation of the conventional binary weighted capacitor bank structure is discussed. Then a novel pseudo-exponential capacitor bank structure is proposed, and an octave bandwidth CMOS LC VCO adopting the proposed capacitor bank structure is implemented to demonstrate significantly linearized coarse tuning characteristics.

II. TUNING RANGE VERSUS TUNING SENSITIVITY

Fig. 1(a) shows the circuit schematic of a CMOS LC VCO considered in this work. The cross-coupled field-effect transistor (FET) pairs M_1 – M_4 generate negative transconductance. The L_1 , L_2 , and C_1 at the common source nodes are for noise filtering. A regulating amplifier reduces the power supply sensitivity and thereby its phase noise contribution. Reference voltage V_{REF} is generated by a replica circuit with a low noise bandgap current. A low pass filter of R_5 and C_5 is employed to further suppress the noise transferred from the regulator. The capacitor bank consists of varactor diodes and a switched metal-insulator-metal (MIM) capacitor array. The varactor diodes are tuned by V_{tune} , and the switched-capacitor bank is tuned by 6-bit digital control code $n\langle 5 : 0 \rangle$.

Fig. 1(b) illustrates typical tuning characteristic when the conventional binary weighted capacitor bank structure is used. Note that the K_{VCO} and $f_{\text{step/code}}$ grows proportionally as the output frequency increases. Here, we quantitatively examine the dependence of the fine and coarse tuning sensitivities

(K_{VCO} and $f_{\text{step/code}}$) on the tuning range. In typical LC VCOs, the output frequency f_o can be simply expressed by

$$f_o = \frac{1}{2\pi\sqrt{L_{\text{tank}}(C_V + C_B)}} \quad (1)$$

where L_{tank} is the tank inductance, C_V is the varactor capacitance, and C_B is the capacitance given by the switched-capacitor bank. In a binary weighted capacitor bank structure, C_B is linearly proportional to the capacitor bank code n as follows:

$$C_B = C_p + \sum_{n=0}^N n \cdot C_{\text{unit}} \quad (2)$$

where C_p is the parasitic capacitance when all the capacitors in the bank are disconnected, C_{unit} is the unit capacitance of the bank, and N is the maximum value of the code n . Assuming $C_{V,\text{max}}$ is negligibly small compared to $C_{B,\text{min}}$ as is the usual case, the VCO tuning range can be approximated to

$$\frac{f_{o,\text{max}}}{f_{o,\text{min}}} = \sqrt{\frac{C_{B,\text{max}}}{C_{B,\text{min}}}} \quad (3)$$

By using the following relations:

$$K_{VCO} = \frac{df_o}{dV_{\text{tune}}} = \frac{df_o}{dC_V} \cdot \frac{dC_V}{dV_{\text{tune}}} \quad (4)$$

$$\frac{f_{\text{step}}}{\text{code}} = \frac{df_o}{dn} \quad (5)$$

the maximum-to-minimum ratio of K_{VCO} and $f_{\text{step/code}}$ are found to be

$$\begin{aligned} \frac{K_{VCO,\text{max}}}{K_{VCO,\text{min}}} &= \frac{f_{\text{step/code,max}}}{f_{\text{step/code,min}}} \\ &= \left(\frac{f_{o,\text{max}}}{f_{o,\text{min}}}\right)^3 = \left(\frac{2 + \text{BW}}{2 - \text{BW}}\right)^3 \end{aligned} \quad (6)$$

in which BW represents the fractional bandwidth given by $2 \times (f_{o,\text{max}} - f_{o,\text{min}})/(f_{o,\text{max}} + f_{o,\text{min}})$.

Equation (6) shows the third-order exponential relationship between the tuning range and tuning sensitivities. A computed result for this dependence is shown in Fig. 2. It clearly exhibits the problematic huge variation of the K_{VCO} and $f_{\text{step/code}}$ as the tuning range grows. For instance, an octave bandwidth tuning will cause K_{VCO} and $f_{\text{step/code}}$ to vary as much as eight times. The variation of the tuning sensitivity will become even severer if larger tuning range is realized. The huge K_{VCO} variation makes difficult optimal design of PLL loop characteristics, possibly leading to critical degradation of phase noise and lock time in some frequency channels. Large K_{VCO} is also likely to cause poor phase noise in VCO. Also, the huge variation of $f_{\text{step/code}}$ will prevent optimal design of automatic frequency calibration (AFC) in a PLL because the number of pulse-counting must be set unnecessarily high enough to detect the smallest frequency step [7]. Therefore, huge variation of K_{VCO} and $f_{\text{step/code}}$ is not desirable for the VCO itself as well as for a PLL employing the VCO.

III. PSEUDO-EXPONENTIAL CAPACITOR BANK STRUCTURE

VCO output frequency is primarily determined by a simple relationship of $1/(2\pi\sqrt{LC})$. To obtain perfectly linear coarse

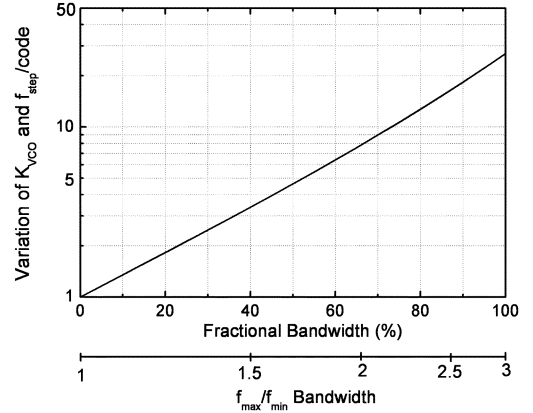


Fig. 2. Variation of the tuning sensitivity (VCO gain [K_{VCO}] and per-code frequency step [$f_{\text{step/code}}$]) against the tuning range in VCO when it employs conventional binary weighted capacitor bank.

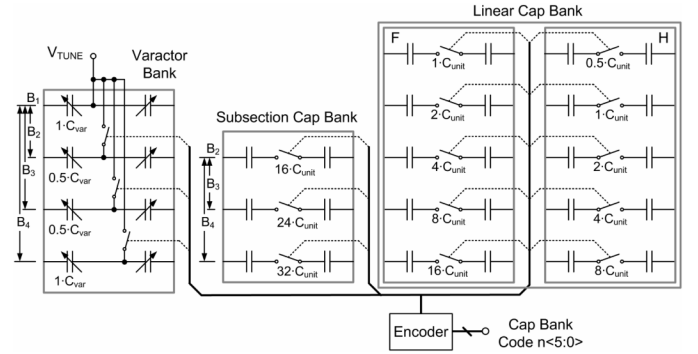


Fig. 3. Pseudo-exponential capacitor bank structure.

tuning characteristics, the total capacitance of capacitor bank must take an exponential form of n^{-2} , rather than a linear form of (2), where n is the cap bank code. This would not be practical due to the unrealistically high ratio of the maximum to minimum capacitances, *e.g.* it reaches 64^2 for the 6-bit capacitor bank in this work. Thus, we decide to realize a pseudo-exponentially varying capacitance bank to mimic the n^{-2} -dependence.

Fig. 3 shows the circuit schematic of the proposed pseudo-exponential capacitor bank where C_{unit} represents a unit metal-insulator-metal (MIM) capacitor and C_{var} represents a unit varactor. The capacitor bank is composed of a subsection cap bank, a linear cap bank, and a varactor bank. The operation of this capacitor bank will be explained in conjunction with the coarse tuning characteristic graphs illustrated in Fig. 4. Fig. 4 conceptually compares the effects of the proposed pseudo-exponential capacitor bank and the conventional binary weighted capacitor bank on the coarse tuning characteristics. First, as shown in Fig. 4(a), total capacitance of a binary weighted capacitor bank varies in a linear way. By contrast, the total capacitance of the proposed capacitor bank varies in a pseudo-exponential way following a piecewise-linear line. The whole region is divided into four subsections $B_1 - B_4$. The number of subsections, which is 4 in this design, is optimally chosen considering coarse tuning linearity and circuit complexity. The piecewise-linear line has different slopes at the four subsections. The different slopes are realized by adequately combining the two binary-weighted cap banks F and H within the linear cap bank, as shown in Fig. 3. It is controlled such that its total capacitance changes linearly in

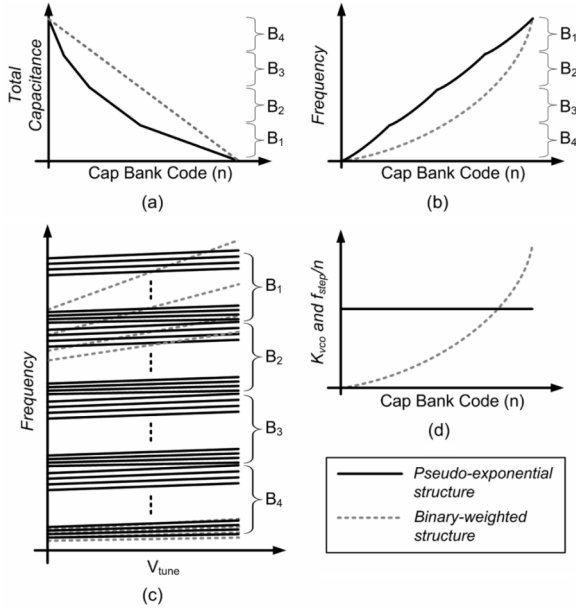


Fig. 4. Effects of the proposed pseudo-exponential capacitor bank structure and the conventional binary-weighted capacitor bank structure. (a) Total capacitance against the cap bank code. (b) Frequency tuning characteristics against the cap bank code at a fixed V_{tune} . (c) Overall coarse tuning characteristics. (d) K_{VCO} and $f_{step}/code$ variation against the cap bank code.

16 steps with different unit capacitances $\{1, 1.5, 2, 3\} \times C_{unit}$ at the subsections $\{B_1, B_2, B_3, B_4\}$, respectively. During the inter-subsection transitions, the total capacitance accumulated by the linear cap bank is absorbed by the subsection cap bank $\{16 \times C_{unit}, 24 \times C_{unit}, \text{ and } 32 \times C_{unit}\}$ and the linear cap bank is reset to zero. In the varactor bank, the varactor size is also adjusted to minimize the K_{VCO} variation with a variable weight of 1, 1.5, 2, and 3 just like in the linear cap bank. Finally the total capacitance of the pseudo-exponential capacitor bank is given by the expression

$$\begin{aligned}
 C_{B1} &= C_{var} + (63 - n) \cdot C_{unit}, & \text{for } n = 63 \sim 48 \\
 C_{B2} &= 1.5 \cdot C_{var} + 16 \cdot C_{unit} + (47 - n) \cdot (1.5 \cdot C_{unit}), & \text{for } n = 47 \sim 32 \\
 C_{B3} &= 2 \cdot C_{var} + 40 \cdot C_{unit} + (31 - n) \cdot (2 \cdot C_{unit}), & \text{for } n = 31 \sim 16 \\
 C_{B4} &= 3 \cdot C_{var} + 72 \cdot C_{unit} + (15 - n) \cdot (3 \cdot C_{unit}), & \text{for } n = 15 \sim 0.
 \end{aligned} \quad (7)$$

Compared to the binary weighted capacitor bank, this pseudo-exponential capacitor bank will greatly linearize the frequency-versus-code characteristics at a fixed V_{tune} , as illustrated in Fig. 4(b). The overall coarse tuning characteristics will be also greatly linearized as shown in Fig. 4(c). As a result, the K_{VCO} and $f_{step}/code$ with respect to the cap bank code can be maintained almost at a constant level as shown in Fig. 4(d).

IV. CIRCUIT DESIGN

A wide-band VCO to cover 940–1724 MHz is designed for an ultrahigh frequency (UHF: 470–862 MHz) transceiver. The VCO frequency is twice higher than the RF frequency because a divide-by-2 is used in final PLL implementation. The circuit schematic of the designed VCO is the same as shown in

Fig. 1(a). The 6-bit pseudo-exponential capacitor bank structure to generate 64 coarse tuning curves is implemented. The number of tuning curves, which is 64 in this design, is optimally chosen by considering two requirements: maintaining low $K_{VCO} (< 100 \text{ MHz/V})$ across the whole tuning range and acquiring at least three overlapping coarse tuning curves at any given frequency. The VCO employing this pseudo-exponential capacitor bank is referred to as VCO-LCT. Meanwhile, the same VCO covering the same tuning range but with a conventional 6-bit binary weighted capacitor bank is also designed for comparison and referred to as VCO-CONV.

The binary weighted structure consists of only 63 of C_{unit} and a single varactor unit. But, according to the design shown in Fig. 3, the pseudo-exponential capacitor bank consists of 72 of C_{unit} in the subsection cap bank, 46.5 of C_{unit} in the linear cap bank, and 3 varactor units. The more devices and longer routings inevitably induce more parasitic capacitances, which makes the minimum capacitance of the pseudo-exponential structure at the lowest cap bank code higher than that of the binary weighted structure. Since the frequency tuning range is determined by the maximum-to-minimum capacitance ratio, the maximum capacitance of the pseudo-exponential structure must be set higher accordingly than the binary weighted structure. As a result, the overall capacitance level of the pseudo-exponential structure is typically higher than that of the binary weighted structure. The capacitor banks in VCO-LCT and VCO-CONV are designed to compensate this complexity difference. The pseudo-exponential structure is designed with C_{unit} of 170 fF, and its total capacitance is simulated to be 12.92–3.19 pF when the capacitor bank code changes from 0 to 63 with V_{tune} fixed at 0.9 V. Under this condition, the tank inductance of the VCO-LCT is chosen to be 1.94 nH to cover the required tuning range. Meanwhile, the binary weighted structure adopts a slightly larger C_{unit} of 210 fF, and its total capacitance is simulated to be 8.09–1.66 pF at $V_{tune} = 0.9 \text{ V}$. Here, the tank inductance of the VCO-CONV is set to be larger 2.64 nH to maintain the same tuning range with the VCO-LCT. Except for the capacitor banks, other parts of both VCOs are designed the same. The noise filtering elements $L_1, L_2,$ and C_2 are 2.1 nH, 2.105 nH, and 13.6 pF, respectively. The simulated output noise of the bandgap reference circuit is 12.2 and 10.9 nV/ $\sqrt{\text{Hz}}$ at 100 kHz and 1 MHz, respectively. The low-pass filter R_5 and C_5 are chosen to be 200 Ω and 7.76 pF, respectively, for which the cutoff frequency is about 102.5 MHz.

V. EXPERIMENTAL RESULTS

The chip was fabricated in a 0.18- μm RF CMOS process. Fig. 5 is the chip micrograph showing the VCO-LCT and VCO-CONV together. The active areas of the VCO-LCT and VCO-CONV are 750×1030 and $720 \times 1030 \mu\text{m}^2$, respectively. The VCO-LCT occupies 4% more area than the VCO-CONV. The active areas of the capacitor banks are $660 \times 195 \mu\text{m}^2$ and $570 \times 160 \mu\text{m}^2$ in the VCO-LCT and VCO-CONV, respectively. The chip is packaged in a 40-pin leadless-plastic chip carrier (LPCC) and tested on a printed circuit board. Both VCOs are tested under the same current dissipation of 6 mA from a 1.8-V supply.

Fig. 6 compares the measured tuning characteristics. The tuning range of the VCO-LCT is 924–1850 MHz (66.7%) and the VCO-CONV shows similar tuning range of 977–1919 MHz

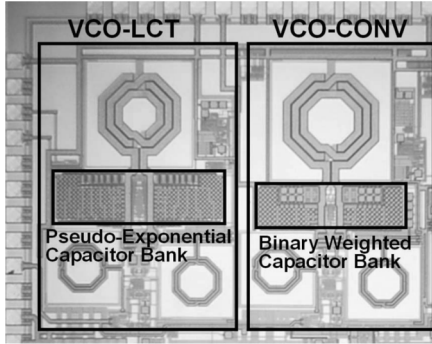


Fig. 5. Chip micrograph.

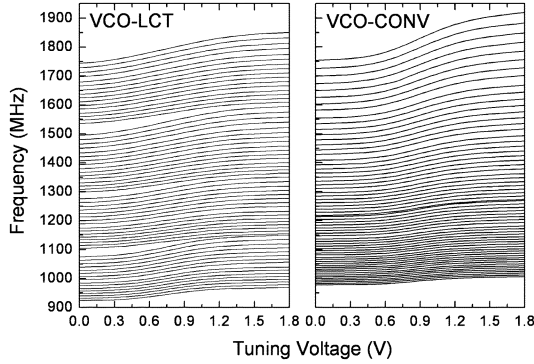
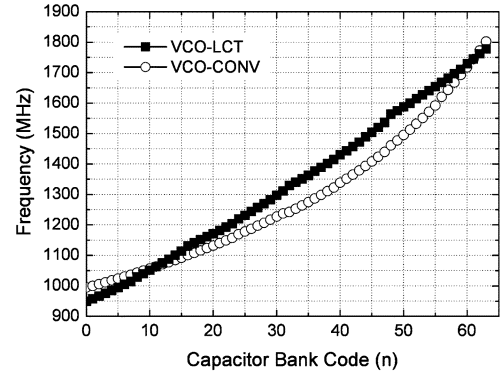


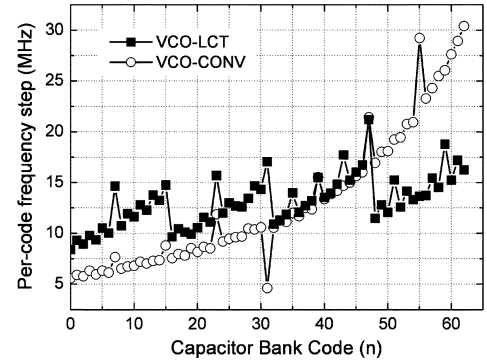
Fig. 6. Measured tuning characteristics of VCO-LCT with the pseudo-exponential capacitor bank and VCO-CONV with the conventional binary weighted capacitor bank.

(65%). Note that the coarse tuning curves of the VCO-LCT are more evenly spaced than those of the VCO-CONV, as expected in Fig. 4(c). The coarse tuning characteristics of both VCOs are characterized and compared in Fig. 7. Fig. 7(a) shows the frequency tuning characteristics at a fixed V_{tune} of 0.9 V. As anticipated in Fig. 4(b), the tuning curve of the VCO-LCT is closer to a straight line than that of the VCO-CONV. The four subsections and the code boundaries at 15, 31 and 47 are clearly visible across the total tuning range of the VCO-LCT. The $f_{\text{step}}/\text{code}$ and K_{VCO} are compared in Fig. 7(b) and (c), respectively. The $f_{\text{step}}/\text{code}$ for the VCO-CONV varies in the range of 5.5–31 MHz/code (560% variation). But for the VCO-LCT, the variation is reduced to 8.4–22.7 MHz/code (270% variation). It is 2.1-times reduction. In addition, the K_{VCO} for the VCO-CONV varies from 33.6 to 160.7 MHz/V (478% variation), while its variation is reduced to 45.2–79 MHz/V (175% variation) for the VCO-LCT. It corresponds to 2.7-times reduction. These tuning sensitivities are found to be remarkably constant compared to the recent state-of-the-art wide-band CMOS VCOs [2], [4].

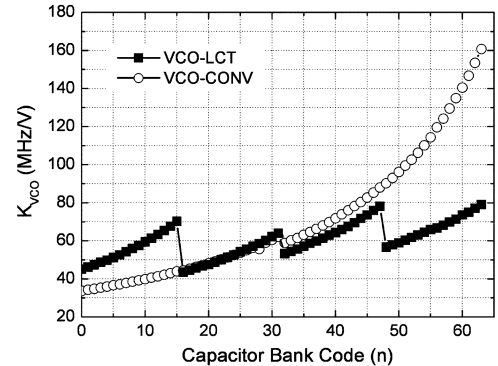
Fig. 8 shows the output spectrum and phase noise measurement results at the high end of the tuning range, in which the output frequency is 1.752 GHz. The phase noise is -94.8 dBc/Hz at 100-kHz offset and -127.1 dBc/Hz at 1-MHz offset. At the low end of the tuning range when the output frequency is 969 MHz, the phase noise is measured to be -109.6 and -128.6 dBc/Hz at 100-kHz and 1-MHz offsets, respectively. For comparison, the phase noises of the VCO-CONV were also measured and found to be very comparable with those of the VCO-LCT. At the high end of the



(a)



(b)



(c)

Fig. 7. Measured coarse tuning characteristics of the VCOs with the pseudo-exponential capacitor bank (VCO-LCT) and the conventional binary weighted capacitor bank (VCO-CONV). (a) Frequency tuning characteristic at a fixed V_{tune} of 0.9 V. (b) Frequency step per a capacitor bank code. (c) VCO gain (K_{VCO})

tuning range, the phase noises were -95.5 dBc/Hz at 100-kHz offset and -128.5 dBc/Hz at 1-MHz offset. At the low end of the tuning range, they were -108.2 dBc/Hz at 100-kHz offset and -128.1 dBc/Hz at 1-MHz offset. Table I summarizes the measured performances of the VCO-LCT and VCO-CONV. The VCO-LCT performances are compared with other recently published wide-band CMOS VCOs [2], [5], [6], [8] in Table II, in which FoM represents the widely used VCO figure-of-merit given by

$$\text{FoM} = \mathcal{L}(\Delta f) - 20 \cdot \log\left(\frac{f_o}{\Delta f}\right) + 10 \cdot \log\left(\frac{P_{\text{diss}}}{1\text{ mW}}\right) \quad (8)$$

where L is the measured phase noise, Δf is the offset frequency, f_o is the oscillation frequency, and P_{diss} is the core power dissipation.

TABLE I
VCO MEASUREMENT SUMMARY

	Tuning Range (MHz)	Bandwidth (%)	K_{VCO} Variation (MHz/V)	$f_{step}/code$ Variation (MHz/code)	Phase Noise (dBc/Hz)		Capacitor Bank Structure
					$f_o=969$ MHz @ 100kHz / 1MHz offset	$f_o=1752$ MHz @ 100kHz / 1MHz offset	
VCO-LCT	924 ~ 1850	66.7	45.2 ~ 79 (175 %)	8.4 ~ 22.7 (270 %)	-109.6 / -128.6	-94.8 / -127.1	Pseudo-Exponential
VCO-CONV	977 ~ 1919	65.1	33.6 ~ 160.7 (478 %)	5.5 ~ 31 (560 %)	-108.2 / -128.1	-95.5 / -128.5	Binary Weighted

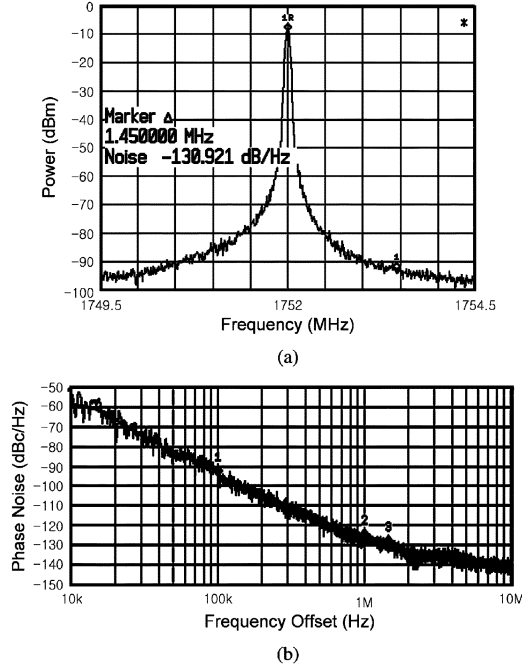


Fig. 8. (a) VCO output spectrum and (b) phase noise measured at the output frequency of 1.752 GHz.

TABLE II
WIDE-BAND VCO COMPARISON

	This Work	[5]	[6]	[8]	[2]
Technology	0.18 μ m CMOS	0.13 μ m CMOS	0.13 μ m CMOS	0.13 μ m CMOS	0.18 μ m CMOS
Implemented Coarse Tuning Linearization Techniques	Both K_{VCO} and $f_{step}/code$	K_{VCO} only	K_{VCO} only	K_{VCO} only	None
Tuning Range (GHz)	0.924 ~ 1.85	3.1 ~ 5.2	3.31 ~ 4.83	1.661 ~ 1.945	1.14 ~ 2.46
Bandwidth (%)	66.7	50.6	37.3	15.8	73.3
Phase Noise (dBc/Hz) ($\Delta f=1$ MHz, $f_o=1.752$ GHz)	-127.1	-114.6	-120.7	-128.5	-99.5
FOM (dBc/Hz)	-181.6	-184.9	-185.5	-181.1	-183.2
Power Consumption (mW)	10.8	2.5	10.8	18	2.6-10
Supply Voltage (V)	1.8	1.2	1.8	1.2	1.5

PLL locking tests including the coarse and fine tuning procedures have been successfully carried out. The coarse tuning

process through AFC loop is implemented with the same structure of [7]. Typical search time for the 6-bit code was measured to be less than 70 μ s when a reference frequency is 19.2 MHz. No noticeable differences were observed during the full locking processes of the VCO-LCT and VCO-CONV.

VI. CONCLUSION

We have demonstrated a wide-band CMOS LC VCO employing a novel pseudo-exponential capacitor bank structure. Implemented in 0.18- μ m CMOS, the VCO-LCT has achieved a tuning range of 924–1850 MHz and phase noise of -127.1 dBc/Hz at 1-MHz offset for 1.752-GHz output frequency, while dissipating 10.8 mW at the core. Compared to the VCO-CONV, the VCO-LCT remarkably reduced the variations of K_{VCO} and $f_{step}/code$ by 2.7 and 2.1 times, respectively. The greatly linearized coarse tuning characteristics have proven that the proposed pseudo-exponential capacitor bank structure can be instrumental in implementing wide-band CMOS LC VCOs.

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